a gate spacer laterally abutting said metal-containing gate conductor and located upon an upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

2. The semiconductor structure of claim **1** further comprising an interlevel dielectric material having conductively filled contact vias that extend to the surface of the semiconductor substrate which includes source and drain regions of the at least one MOSFET.

3. The semiconductor structure of claim **2** further comprising a spacer liner present between the gate spacer and the interlevel dielectric material, the metal-containing gate conductor and the upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

4. The semiconductor structure of claim **1** wherein said gate spacer is a low-k dielectric material that has a dielectric constant of less than 4.

5. The semiconductor structure of claim **1** wherein said gate spacer includes a void present in an interior thereof which lowers the effective dielectric constant of the gate spacer.

6. The semiconductor structure of claim **1** wherein said gate dielectric has a first height, said high-k gate dielectric that is present at the gate corners has a second height, and said high-k gate dielectric located directly beneath said metal-containing gate conductor has a third height, wherein said first height is substantially the same as, or greater than, the second height, and said second height is greater than the third height.

7. The semiconductor structure of claim **1** wherein said high-k gate dielectric at said gate corners has increased bonding as compared to said high-k gate dielectric that is located directly beneath said metal-containing gate conductor.

8. The semiconductor structure of claim **1** wherein said high-k gate dielectric comprises one of TiO_2, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, La_2O_3, a perovskite-type oxide, and a silicate or nitride thereof.

9. The semiconductor structure of claim **1** wherein said metal-containing gate conductor is one of a conductive metal, an alloy of a conductive metal, a silicide of a conductive metal and a nitride of a conductive metal.

10. A semiconductor structure comprising:

at least one metal oxide semiconductor field effect transistor (MOSFET) located on a surface of a semiconductor substrate, said at least one MOSFET comprising a gate stack including, from bottom to top, a high-k gate dielectric and a metal-containing gate conductor, said metal-containing gate conductor having gate corners located at a base segment of the metal-containing gate conductor, wherein said metal-containing gate conductor has vertical sidewalls devoid of said high-k gate dielectric except at said gate corners, said high-k gate dielectric at said gate corners has increased bonding as compared to said high-k gate dielectric that is located directly beneath said metal-containing gate conductor;

a gate dielectric laterally abutting said high-k gate dielectric present at said gate corners; and

a gate spacer laterally abutting said metal-containing gate conductor and located upon an upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

11. The semiconductor structure of claim **10** further comprising an interlevel dielectric material having conductively filled contact vias that extend to the surface of the semiconductor substrate which includes source and drain regions of the at least one MOSFET.

12. The semiconductor structure of claim **11** further comprising a spacer liner present between the gate spacer and the interlevel dielectric material, the metal-containing gate conductor and the upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

13. The semiconductor structure of claim **10** wherein said gate spacer is a low-k dielectric material that has a dielectric constant of less than 4.

14. The semiconductor structure of claim **10** wherein said gate spacer includes a void present in an interior thereof which lowers the effective dielectric constant of the gate spacer.

15. The semiconductor structure of claim **10** wherein said gate dielectric has a first height, said high-k gate dielectric that is present at the gate corners has a second height, and said high-k gate dielectric located directly beneath said metal-containing gate conductor has a third height, wherein said first height is substantially the same, as or greater than, the second height, and said second height is greater than the third height.

16. The semiconductor structure of claim **10** wherein said high-k gate dielectric comprises one of TiO_2, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, La_2O_3, a perovskite-type oxide, and a silicate or nitride thereof.

17. The semiconductor structure of claim **10** wherein said metal-containing gate conductor is one of a conductive metal, an alloy of a conductive metal, a silicide of a conductive metal and a nitride of a conductive metal.

18. A semiconductor structure comprising:

at least one metal oxide semiconductor field effect transistor (MOSFET) located on a surface of a semiconductor substrate, said at least one MOSFET comprising a gate stack including, from bottom to top, a high-k gate dielectric and a metal-containing gate conductor, said metal-containing gate conductor having gate corners located at a base segment of the metal-containing gate conductor, wherein said metal-containing gate conductor has vertical sidewalls devoid of said high-k gate dielectric except at said gate corners;

a gate dielectric laterally abutting said high-k gate dielectric present at said gate corners; and

a low-k gate spacer that includes voids in the interior thereof laterally abutting said metal-containing gate conductor and located upon an upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

19. The semiconductor structure of claim **18** further comprising an interlevel dielectric material having conductively filled contact vias that extend to the surface of the semiconductor substrate which includes source and drain regions of the at least one MOSFET.

20. The semiconductor structure of claim **19** further comprising a spacer liner present between the gate spacer and the interlevel dielectric material, the metal-containing gate conductor and the upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

21. The semiconductor structure of claim **18** wherein said gate dielectric has a first height, said high-k gate dielectric that is present at the gate corners has a second height, and said high-k gate dielectric located directly beneath said metal-containing gate conductor has a third height, wherein said